REMARKS

Claims 1-15 and 18 are currently pending. Claims 8 and 10 have been amended by the above to correct a minor typographical error and to clarify claim scope as with respect to claim 10. Applicants respectfully request reconsideration of the present application.

Summary of Claimed Subject Matter

As recited in claim 1, the presently claimed invention is directed to a method of manufacturing a semiconductor device. The method includes steps (a) through (e). The first step involves sequentially stacking a semiconductor layer 33, a mask layer 35, and a metal layer 39, on a substrate 31 as shown in the exemplary embodiment of Figure 3A, for instance. Step (b) involves anodizing the metal layer 39 to transform the metal layer into a metal oxide layer 39 to include a plurality of nanoholes such as shown in Figure 3B. Step (c) involves etching the mask layer 35 using the metal oxide layer 39A as an etch mask until the nanoholes are extended to the surface of the semiconductor layer, as shown in Figure 3C. The metal oxide layer is then removed by etching as shown in Figure 3D. Thereafter, as shown in the exemplary embodiment of Figure 3E, the semiconductor layer is regrown to completely fill the nanoholes in the mask layer and extend above the mask layer to cover the mask layer between the nanoholes. As shown in Figure 3E, the semiconductor layer covers all the mask layer, as recited in claim 18.

Claim 2 recites that each of the nanoholes has a diameter of 10 to 500 nm and claim 3 recites that each of the nanoholes occupies less than 50% of the entire area. The mask layer has a thickness of 50 to 500 nm as recited in claim 4.

As recited in claim 5, the semiconductor layer has a lattice constant which is different from the lattice constant of the substrate. Claim 6 specifies that the substrate is made of one of an inorganic crystal including sapphire, Si, SiC, $MaAl_2O_4$, $NdGaO_3$, $LiGaO_2$, ZnO, or Mao, a III-V group compound semiconductor including GaP or GaAs, and a III group nitride semiconductor including GaN. Claim 7 specifies that the semiconductor layer is a nitride semiconductor and claim 8 further specifies that it is made of one of GaN, InGaN, AlGaN, AlInGaN and InGaNAs.

Claim 9 recites that the mask layer can be made of a polycrystalline semiconductor, dielectric material or a metal and claim 10 further specifies that the polycrystalline semiconductor layer is one of polysilicon and polycrystalline nitride. Claim 11 recites the mask layer is one of silicon oxide, titanium oxide or zirconium oxide, whereas claim 12 recites that the mask layer is a metal and has a melting point of 1200°C or higher. Claim 13 specifies that the metal of the mask layer is one of titanium and tungsten whereas claim 14 recites that the metal layer is formed of aluminum. Claim 15 recites that the etching process is a dry etch process.

Grounds of Rejection

Claim 1-15 and 18 stand rejected under 35 U.S.C. § 103 as allegedly being unpatentable over the Tsakalakos et al. published patent application (US 2004/0077156) in combination with the Zhang et al. published patent application (US 2003/0010971). Applicants respectfully traverse this rejection.

Tsakalakos et al. Published Patent Application

Tsakalakos et al. published patent application discloses the use of a copolymer thin film which undergoes a selective etching process wherein the first component is strongly resistant to a particular reactive etching process and the second component of the block copolymer is easily etched away. This results in a series of nanoholes. A thin film 204 is grown over the exposed surface 206 to promote lateral epitaxial vertical and lateral growth. As mentioned during the personal interview conducted on June 23, 2006 and repeated in the Amendment of July 21, 2006 at page 7, a problem with a hypothetical combination proposed in the Office Action is that the intended purpose or function of one or both of the applied references is destroyed by their combination. This indicates that a *prima facie* case of obviousness has not been established. *In re Gordon* 733, Fed. 2nd 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). In this instance, because the Zhang et al. published patent application discloses that its purpose is to create electrical devices in the form of nanoscale MOSFETs in the nanopores it forms, it would be inappropriate to suggest that it would be obvious to one of ordinary skill in the art to find motivation for the hypothetical combination despite the destruction of the core features and function of the Zhang et al. disclosure. Hence, the combination is inappropriate regardless of whether one views the Zhang et al. published patent application or the Tsakalakos published patent application as being the primary reference.

Additionally, the block copolymer films of the Tsakalakos published patent application, which creates the nanoscale patterns, requires only an etching process. To accept the hypothetical combination proposed in the Office Action, one skilled in the art would have to adopt a relatively complex process as disclosed in the Zhang et al. published patent application. It is respectfully submitted that one skilled in the

art would not move from a relatively straightforward single step process to a relatively complex multistep process absent some compelling reasons or advantages to be gained, the teaching of which is not present in the applied art. Stated in a different light, the approach taken by the Tsakalakos et al. published patent application and the Zhang et al. published patent application are neither equivalent nor would it be reasonable to assume that one of ordinary skill in the art would opt for the more complex process without their being additional reasons not apparent in the record. In other words, the prior art does not supply motivation for a hypothetical combination which would result in the present application but instead it is respectfully submitted that the Office must have relied on hindsight in reconstructing the Applicants' invention using Applicants' own teachings and claims as a template to pick and choose features from the applied art.

Claims 12 and 13

As stated previously, the mask layer of claim 12 is a metal that has a melting point of 1200°C or higher. Claim 13 recites that the metal of the mask layer is one of titanium and tungsten. It should be noted that recitation of the metal is supported by the metal layer 39 in the exemplary embodiment, which is to be anodized into a nanoporous metal oxide 39A and used as an etch mask for etching a lower layer. Instead, these claims are directed to the mask layer as supported by the mask layer 35 of the exemplary embodiment which is used as a regrowth mask for selectively removing the semiconductor after removing the nanoporous metal oxide layer 39A.

Applicants respectfully submit that the Office may have mistook the metal of claims 12 and 13 to be the metal layer, as recited in claim 1. Applicants mention this

because the Zhang et al. patent does not disclose or suggest a metal having a melting point of 1200°C or higher or titanium of tungsten that can be used as a mask layer for selective regrowth of a semiconductor after removing the nanoporous metal oxide. Specifically, paragraph [0028] of the Zhang patent mentions a titanium layer, but it is not a mask layer for selectively regrowing a semiconductor after removing the metal oxide layer (AAO) 10', but only a thin barrier layer for improving adhesion between the two layers 20', 30 and facilitating an anodization process. *See* page 4, paragraph [0028] and Figures 2A-2B of the Zhang publication. In the process shown in Figures 2A, 2C of the Zhang published patent application, the Zhang disclosure does not use a mask layer separate from the AAO film 10'. The Zhang process uses the AAO film 10' itself as a mask layer for selective growth to form silicon pillars 32. *See* also paragraphs [0028] - [0029] of the Zhang published patent.

In another process shown in Figures 5A-5E, the Zhang published patent application uses the layer 96 as a growth mask template. However, the mask layer 96 is an electrically insulating layer (*e.g.*, SiO_2). *See* page 6, paragraphs [0040] and [0041] of the Zhang published patent application. The titanium layer on the mask layer 96 is not a growth mask, but only a barrier layer (an anodization). The titanium metal layer itself cannot be used as a growth mask. In addition, the layer 96 for a growth mask should not be a metal but an insulator. This is because the material of the layer 96 between the channels must have a wide band gap, *i.e.*, a wide enough band gap to treat the lateral coupling of quantum dots 90a, 90b, as negligible. *See* paragraph [0042] of the Zhang published patent application.

Conclusion

In light of the foregoing, Applicants respectfully request reconsideration and allowance of the above-captioned application. Should any residual issues exist, the Examiner is invited to contact the undersigned at the number listed below.

Respectfully submitted,

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Date: November 9, 2006

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